with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

matched-filter means, coupled to said spread-spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to a detected match having a correspondence between the header-chip-sequence signal and the first impulse response above a header threshold, a header detection signal having [a] an in-phase-header amplitude and a quadrature-phase-header amplitude and a respective chip location;

header-memory means, coupled to said matched-filter means, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal and the respective chip location of each header-detection signal;

said matched-filter means having a second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting,

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4

at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, a data-detection signal having [a] an in-phase-data amplitude and a quadrature-phase data amplitude; and

combining means, coupled to said header-memory means and to said matched-filter means, for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal at each corresponding chip location, respectively, thereby generating a plurality of in-phase-weighted elements and a plurality of quadrature-phase-weighted elements for each data symbol within the data portion, and for combining the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements of a respective data symbol as a sum signal of the respective data symbol.

2. (Once Amended) The multipath-combining subsystem as set forth in claim 1 wherein said combining means includes:

product means for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-date amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating [a] the plurality of in-phase-weighted elements and

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the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

4. (Once Amended) The multipath-combining subsystem as set forth in claim 3 wherein said combining means includes:

product means for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating [a] the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding

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each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

7. (Once Amended) The multipath-combining subsystem as set forth in claim 1 wherein said matched-filter means includes:

a header-matched filter, coupled to said spread-spectrum receiver, having the first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within each packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, and for outputting, responsive to a detected match having a level of correspondence above the header threshold, the header-detection signal having [a] the in-phase-header amplitude and the quadrature-phase-header amplitude and a respective chip location; and

a data-matched filter, having the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, the in-phase-data amplitude and the quadrature-phase-data amplitude of the data-detection signal.

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8. (Once Amended) The multipath-combining subsystem as set forth in claim 1 wherein said matched-filter means includes:

a programmable-matched filter, coupled to said spread-spectrum receiver, having the first impulse response initially matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within each packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, and for outputting, responsive to a detected match having a level of correspondence above the header threshold, a header detection signal having [a] the in-phase-header amplitude and the quadrature-phase-header amplitude and a respective chip location; and

said programmable-matched filter, having the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, the in-phase-data amplitude and the quadrature-phase-date amplitude of the data-detection signal.

9. (Once Amended) The multipath-combining subsystem as set forth in claim 7 or 8 wherein said combining means includes:

product means for multiplying the header amplitude of

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each header-detection signal by the data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating [a] the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

10. (Once Amended) A multipath-combining subsystem for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

a header-matched filter, coupled to said spread-

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spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to a detected match having a correspondence between the header-chip-sequence signal and the first impulse response above a header threshold, a header detection signal having [a] an in-phase-header amplitude and a quadrature-phase-header amplitude and a respective chip location;

a header memory, coupled to said header-matched filter, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal and the respective chip location of each header-detection signal;

a symbol-matched filter, having a second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, a data-detection signal having [a] an in-

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phase-data amplitude and a quadrature-phase data amplitude;

a header-timing circuit, coupled to an output of said header-matched filter, for detecting, from a plurality of header-detection signals, a strongest header-detection signal and, responsive to the strongest header-detection signal, for outputting a packet-start signal;

product means, coupled to an output of said header-matched filter and to an output of said header-timing circuit, for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating [a] the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

adding means, coupled to an output of said product means, for adding the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for a respective data symbol to generate a sum signal of the respective data symbol;

a combiner memory, coupled to an output of said adding means, for storing the sum signal; and

a data demodulator, coupled to said combiner memory, for detecting data from the sum signal.

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11. (Once Amended) A multipath-combining subsystem for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

a programmable-matched filter, coupled to said spread-spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to each detected match above a header threshold, [a] an in-phase-header amplitude and a quadrature-phase-header amplitude and a respective chip location;

a header memory, coupled to said programmable-matched filter, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude and the respective chip

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location of each header-detection signal;

a header-timing circuit, coupled to an output of said programmable-matched filter, for detecting, from a plurality of header-detection signals, a strongest header-detection signal and, responsive to the strongest header-detection signal, for outputting a packet-start signal;

said programmable-matched filter, responsive to the packet-start signal, for changing the first impulse response to a second impulse response, the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each in-phase-header-detection signal and of each quadrature-phase-header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, a data-detection signal having [a] an in-phase-data amplitude and a quadrature-phase data amplitude;

product means, coupled to an output of said header-matched filter and to an output of said header-timing circuit, for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating [a] the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data

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symbol of the data-symbol-sequence signal;

adding means, coupled to an output of said product means, for adding the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for a respective data symbol to generate a sum signal of the respective data symbol;

a combiner memory, coupled to an output of said adding means, for storing the sum signal; and

a data demodulator, coupled to said combiner memory, for detecting data from the sum signal.

12. (Once Amended) A multipath-combining method for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining method comprising the steps of:

a. detecting, with a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, within a packet and for each path, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of

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the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal;

b. outputting, in response to each detected match above a header threshold, a header-detection signal having [a] an in-phase-header amplitude and a quadrature=-phase-header amplitude and a respective chip location;

c. storing the in-phase-header amplitude and the quadrature-phase-header amplitude and the respective chip location of each header-detection signal;

d. detecting, with a second impulse response matched to the data-chip-sequence signal embedded in the data portion of the spread-spectrum signal, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response;

e. outputting, responsive to each detected match, a data-detection signal having [a] an in-phase-data amplitude and a quadrature-phase-data amplitude;

f. multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal with the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection-signal at each corresponding chip location, respectively, thereby generating a plurality of in-phase-weighted elements and a plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal; and

g. adding the plurality of in-phase-weighted

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